

SED1190

CMOS LCD 64-COMMON DRIVERS

DESCRIPTION

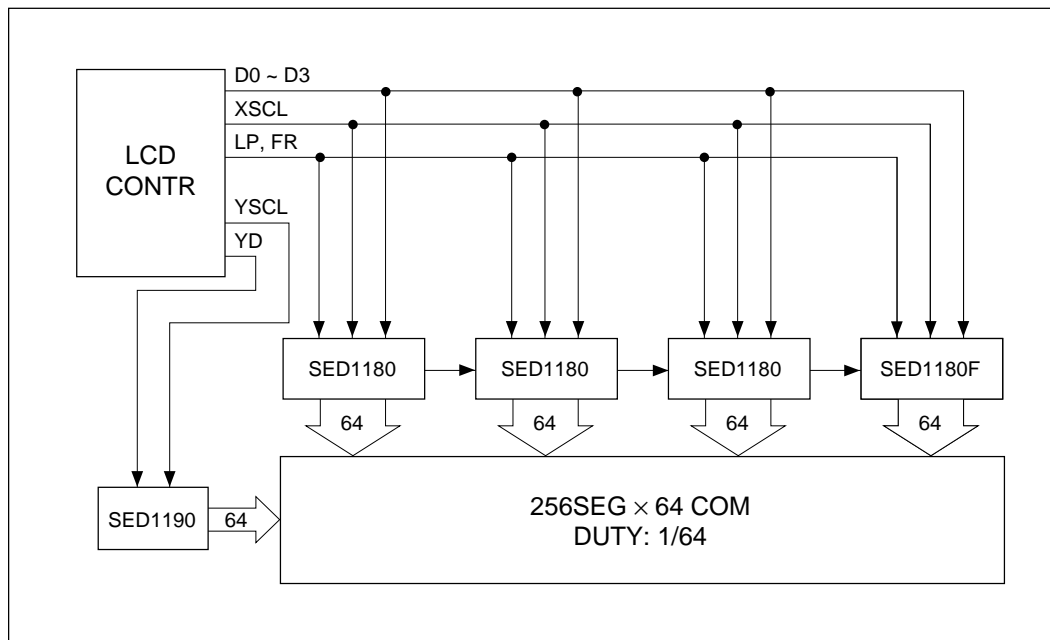
The SED1190 is a dot matrix LCD common (row) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI uses two serially connected, 32-bit shift registers to hold the display data, and level shifter converts the TTL level 64-bit parallel data from the shift registers to levels suitable for use by the LCD drive circuitry. The SED1190 generates common drive signals using the voltages supplied to LCD drive voltages pins.

The SED1190 is used in conjunction with the SED1180 (64-bit row driver) to drive a large capacity dot matrix LCD panel.

FEATURES

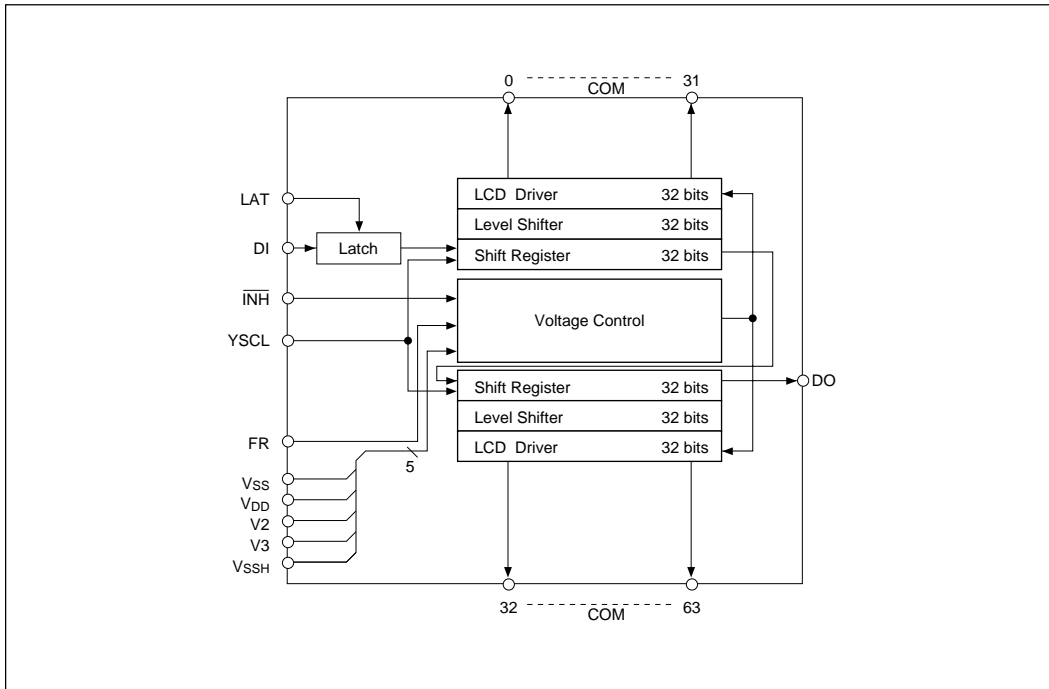
- Low-power CMOS technology
- 64-bit common (row) driver
- Display blanking
- Duty cycle: 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage: -14V to -25V
- Supply voltage: 5.0V ±10%
- Package: QFP1-80 pin (F0A)
QFP5-80 pin (F5A)
DIE: Al pad chip (D0A)

SYSTEM BLOCK DIAGRAM

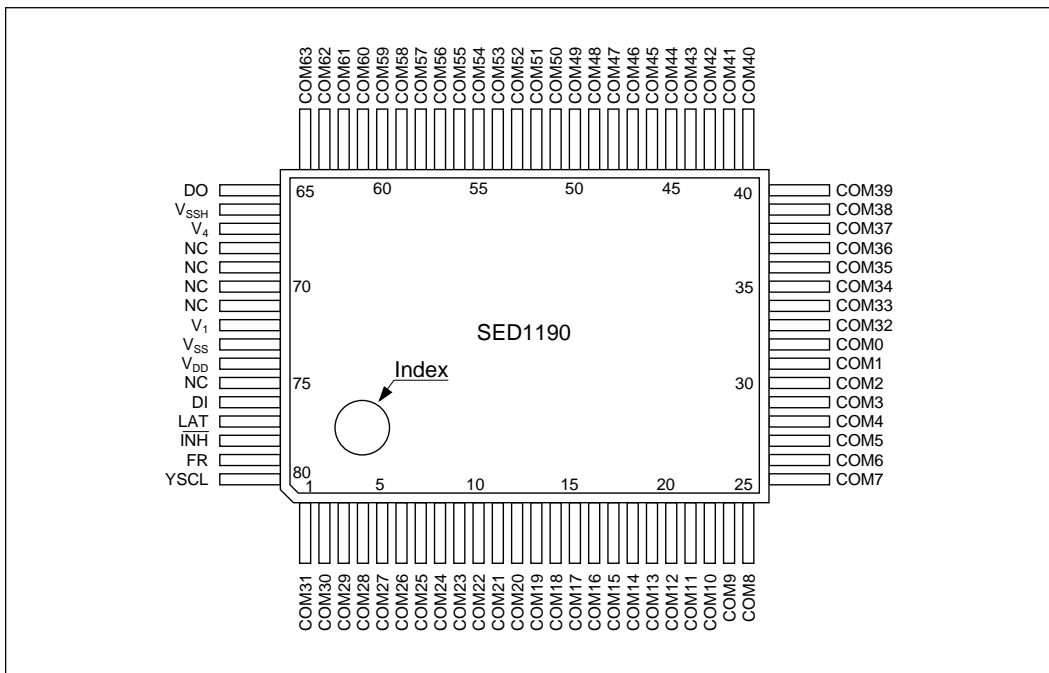


SED1190

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	VSSH
7	COM25	27	COM 5	47	COM46	67	V4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V1
13	COM19	33	COM32	53	COM52	73	Vss
14	COM18	34	COM33	54	COM53	74	VDD
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	LAT
18	COM14	38	COM37	58	COM57	78	INH
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	YSCL

NC = Not connected

■ PIN DESCRIPTION

Pin Name	Function											
COM0 to COM63	LCD common drive outputs											
DI	Serial data input											
LAT	Transparent latch control input:											
	<table border="1"> <thead> <tr> <th>LAT</th> <th>DI</th> <th>DI latch output</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>X</td> <td>DI latch</td> </tr> </tbody> </table>	LAT	DI	DI latch output	H	H	H	L	L	L	X	DI latch
	LAT	DI	DI latch output									
	H	H	H									
L		L										
L	X	DI latch										
DO	Serial data output											
YSCL	Serial data shift clock. Data is shifted through the controller on the falling edge of this clock											
FR	LCD AC-drive signal input											
INH	Active-low blanking input											
VDD, VSS	Logic power supply inputs											
V1, V4, VSSH	LCD drive power inputs VDD ≥ V1 ≥ V4 ≥ VSSH											

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{SS}	-7.0 to +0.3	V
Supply voltage (2)	V _{SSH}	-28.0 to +0.3	V
	V1, V4		
Input voltage	V _I	V _{SS} -0.3 to +0.3	V
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C
Soldering temperature and time	T _{sol}	260, 10	°C, s

Notes:

1. All voltages referenced to a V_{DD} of 0 V.
2. V1 and V4 must satisfy the relationship $V_{DD} \geq V1, V4 \geq V_{SSH}$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

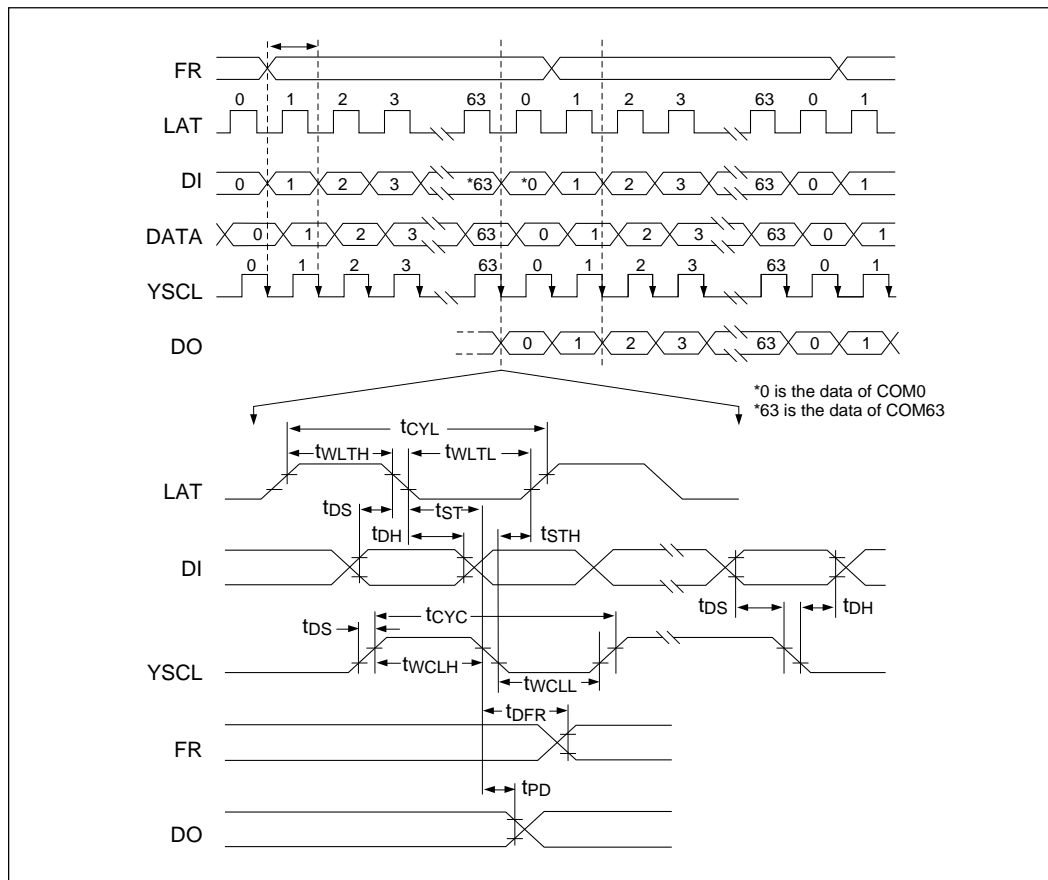
● DC Characteristics

(V_{DD} = 0V, V_{SS} = -5.0 V ±10%, T_a = -20 to 75°C)

Parameter	Symbol	Conditions	Rating			Unit	
			Min	Typ	Max		
Supply voltage (1)	V _{SS}		-5.5	-5.0	-4.5	V	
Supply voltage (2)	V ₁		V _{SSH}	—	V _{DD}	V	
	V ₄		V _{SSH}	—	V _{DD}	V	
	V _{SSH}	Recommended V _{SSH}	-25.0	—	-14.0	V	
		Operable V _{SSH} (see note)	-25.0	—	-5.0	V	
High level input voltage	V _{IH}		0.2V _{SS}	—	V _{DD} +0.3	V	
Low level input voltage	V _{IL}		V _{SS} -0.3	—	0.8V _{SS}	V	
High level output voltage	V _{OH}	I _{OH} = -0.6 mA	-0.4	—	—	V	
Low level output voltage	V _{OL}	I _{OL} = 0.6 mA	—	—	V _{SS} +0.4	V	
Input leakage current	I _{LI}	0 V ≥ V _I ≥ V _{SS}	—	0.05	2.0	μA	
Output leakage current	I _{LO}	0 V ≥ V _O ≥ V _{SS}	—	0.05	5.0	μA	
Shift clock	YSCL		—	—	2.5	MHz	
Frame signal	FR		—	1/60	—	s	
Input capacitance	C _I	T _a = 25°C	—	5.0	8.0	pF	
Common output on resistance	R _{COM}	V _{OH} = V _{DD} -0.5 V V _{OL} = V _{SSH} +0.5 V COM bit	V _{SSH} = -20.0 V	—	0.8	1.0	kΩ
			V _{SSH} = -14.0 V	—	0.9	1.3	
			V _{SSH} = -9.0 V	—	1.3	2.0	
			V _{SSH} = -5.0 V	—	3.0	30.0	
Quiescent current	I _Q	SED 1190 V _{SSH} = -25 V, V _{SSH} = -5.5 V, V _I = V _{DD}	—	0.05	30	μA	
Operating current for the logic	I _{SS}	FR cycle = 16.7 ms	V _{SS} = -5.0 V, V _{IH} = V _{DD} , V _{IL} = V _{SS} , YSCL cycle = 130 μs (duty 50%), All "H" output terminals are opened at every data input all 1/128 duty.	—	3.0	8.0	μA
Operating current for LCD	I _{SSH}	FR cycle = 16.7 ms	V _{SS} = -4.5 V, V ₁ = -2.0 V, V ₄ = -18.0 V, YSCL cycle = 130 μs (duty 50%), All "H" output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	μA
Pull up MOS current	-I _p	V _{SS} = -5.0 V, V _{IL} = -5.0 V Applicable to LAT input terminals	10.0	25.0	50.0	μA	

Note: Error free operation is guaranteed in this range but the output resistance of the LCD drivers is higher than in the recommended operating range. It is suggested that the driver is tested with the target LCD panel to determine if performance is acceptable.

- AC Electrical Characteristics
 - I/O Signal Timing

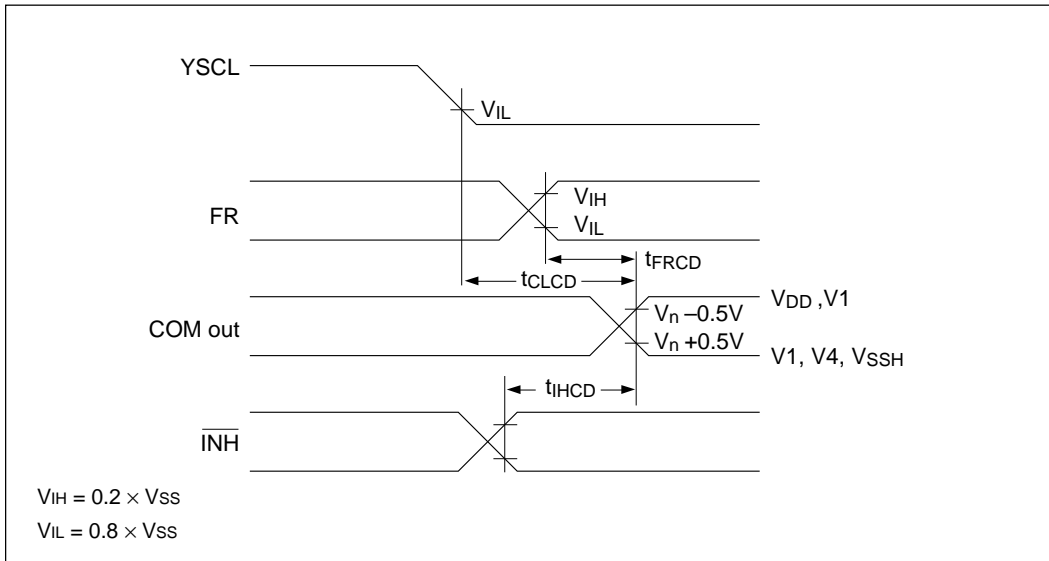


$V_{DD} = 0V, V_{SS} = -5.0V \pm 10\%, T_a = -20 \text{ to } 75^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch pulse cycle time	tCYL	—	400	—	—	ns
Latch pulse "H" width	tWLTH	—	180	—	—	ns
Latch pulse "L" width	tWLL	—	180	—	—	ns
Shift clock cycle time	tCYC	—	400	—	—	ns
Shift clock "H" time	twCLH	—	110	—	—	ns
Shift clock "L" time	twCLL	—	110 (240)	—	—	ns
Data setup time	tDS	—	100 (70)	—	—	ns
Data hold time	tDH	—	30	—	—	ns
Data shift timing	tST	—	0	—	—	ns
Data shift hold time	tSTH	—	125	—	—	ns
Permissible frame signal delay	tDFR	—	-500	0	500	ns
Input signal rise time	tr	—	—	—	*	ns
Input signal fall time	tf	—	—	—	*	ns
Data output delay time	tPD	CL = 15pF	30	—	170	ns

* tr, tf = (tCYL - tWLH - tWLL) / 2 where tf ≥ 50ns.

● Common Drive

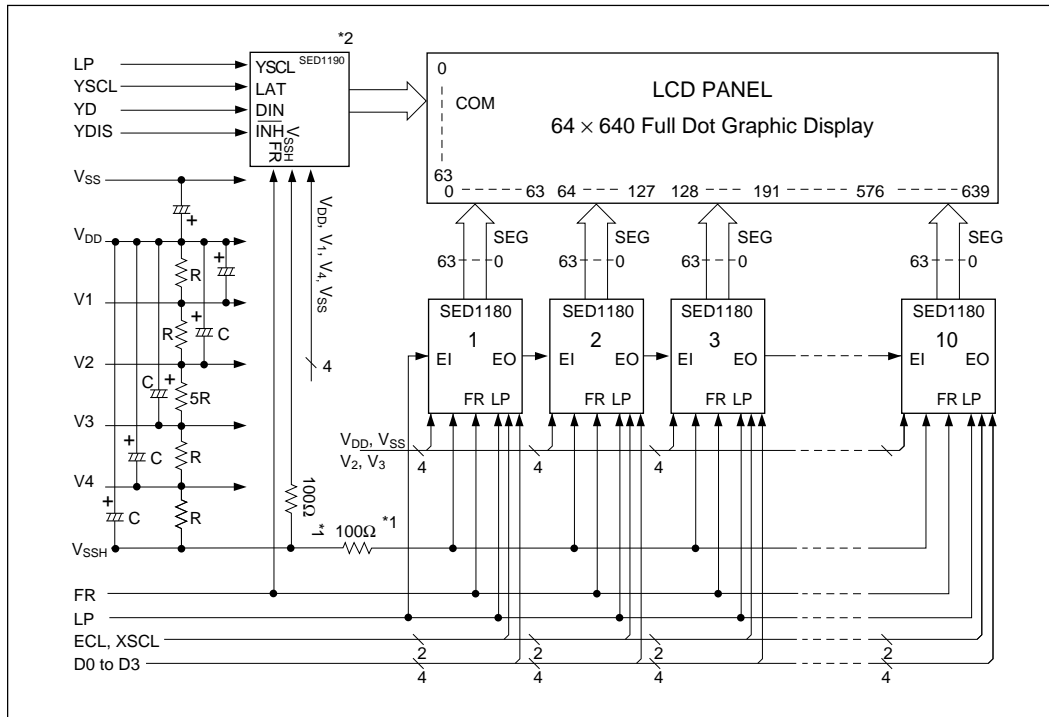


$V_{DD} = 0V, V_{SS} = -5.0V \pm 10\%, T_a = -20 \text{ to } 75^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL – COM output delay time	t_{CLCD}	$V_{SSH} = -14.0 \text{ to } -25.0V$ $C_L = 100pF$	—	—	3.0	μs
RF – COM output delay time	t_{FRCD}		—	—	3.0	μs
INH – COM output delay time	t_{IHCD}		—	—	3.0	μs

■ EXAMPLE OF APPLICATION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass Vss and Vssh with capacitors of at least 0.01 μF