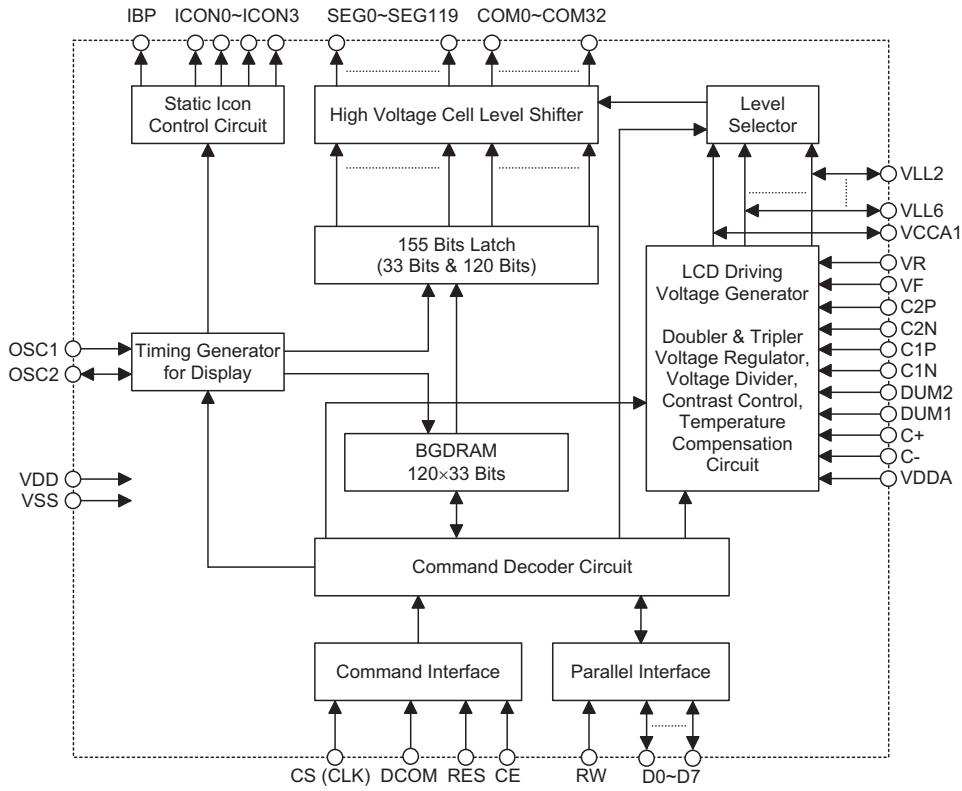
Features

- Operating voltage: 2.4V~3.5V
- 33 common/120 segment LCD driver output
- 33×120=3960 bits capacity of built-in graphic display data RAM (BGDRAM)
- Master and slave mode available for multi-chip operation
- 8-bit Parallel interface with general MCU
- On-chip oscillator circuit for display clock, external clock can also be used
- Selectable multiplex ratio: 1/16, 1/32, 1/33
- Selectable bias ratio: 1/5 or 1/7
- External driving circuit for external bias supply
- On-chip selectable voltage doublers and tripler
- Wide range of operating temperature: –30°C to 85°C
- S/W controlled electronic contrast control function (16 levels)
- External contrast control
- Low power icon mode driven by com32
- Four static icon driver circuit
- High accuracy voltage regulator with temperature coefficient (0.00%, –0.18%, –0.22%, –0.35%)
- Low power consumption
  - Read/write mode 170μA (Typical)
  - Display mode 160μA (Typical)
  - Standby mode 15μA (Typical; Display off; internal oscillator enable)
  - Standby mode < 1μA (Typical; Display off; external oscillator enable)
- CMOS process
- TCP available

General Description

The HT0610 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It has 33 common and 120 segment driver circuits. This chip is connected directly to an MCU, accepts 8-bit parallel display data and stores an on-chip graphic display data RAM (BGDRAM) of 33×120 bits. It provides a high-flexible display section due to the one-to-one correspondence between BGDRAM bits and LCD panel pixels. It performs BGDRAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive an LCD, it is possible to make a display system with minimal components.

Block Diagram



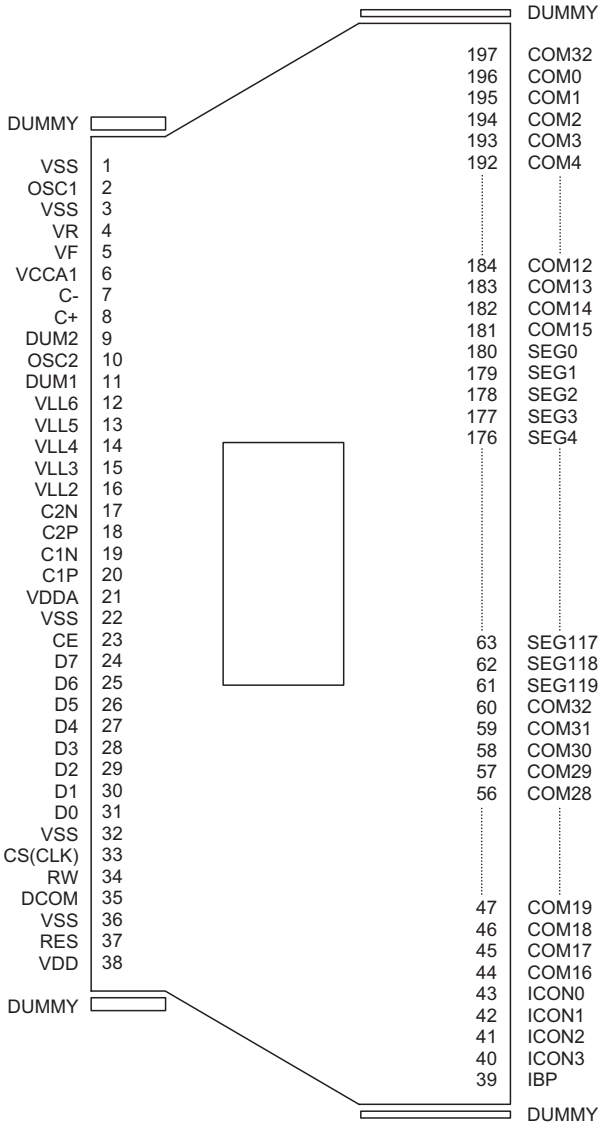
Operation of LCD Driver

Description of block diagram module

Block	Description
Command Decoder and Command Interface	This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the DCOM pin. If DCOM High, then data is written to BGDRAM (Built-in Graphic Display data RAM) . DCOM pin Low indicates that the input at D0~D7 is interpreted as a Command. CE is the master chip selection signal . A High input enable the input lines ready to sample signals. RES pin of same function as Power On Reset (POR). Once RES received the reset signal, all internal circuitry will back to its initial status. Refer to Command Description section for more information.
Parallel Interface	The parallel interface consists of 8 bi-directional data lines (D0~D7),RW, and CS. The RW input High indicates a read operation from the BGDRAM . RW input Low indicates a write to BGDRAM or Internal Command Registers depending on the status of DCOM pin input. The CS input serves as data latch signal (clock).
Built-in Graphic Display data RAM (BGDRAM)	The BGDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the BGDRAM is determined by number of row times the number of column (120×33 =3960 bits). Figure as follow is a description of the BGDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided
Display Timing Generator	This module is an on chip low power RC oscillator circuitry. The oscillator frequency can be selected in the range of 15kHz to 50kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Block	Description
Static Icon Control Circuit	This module generates the LCD waveform of the 4 annunciators and IBP signal. The four independent static icons are enabled by software command. Icon signals are also controlled by oscillator circuit, too.
LCD Driving Voltage Generator	This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of: • Voltage doubler and voltage tripler To generate the VCCA1 voltage. Either doubler or tripler can be enabled. • Voltage regulator Feedback gain control for initial LCD voltage. It can also be used with external contrast control. • Voltage divider Divide the LCD display voltage (VLL2~VLL6) from the regulator output. This is low power consumption circuit, which can save the most display current compare with traditional resistor ladder method. • Bias Ratio Selection circuitry Software control of 1/5 and 1/7 bias ratios to match the characteristic of LCD panel. • Self adjust temperature compensation circuitry Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. • Contrast Control Block Software control of 16 voltage levels of LCD voltage. • External Contrast Control By adjusting the gain control resistors connected externally, the contrast can be varied. All blocks can be individually turned off if external voltage generator is employed.
120 Bit Latch/33 Bit Latch	153 bit long registers, which carry the display signal information. First 33 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.
Level Selector	Level selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.
HV Buffer Cell (Level Shifter)	HV Buffer Cell works as a level shifter that translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Pin Assignment



Pin Description

Pin Name	I/O	Description
VDD	I	VDD is the positive supply to the digital control circuit and other circuitry in LCD bias voltage generator (Must have same voltage level with VDDA)
RES	I	Active low reset pin; reset all internal status of circuit (Same as power on reset)
VSS	I	VSS is ground
DCOM	I	If pull this pin ″High″ then D0~D7 bi-direction bus is used for data transferring; If DCOM pin is ″Low″ then D0~D7 bi-direction bus is used for command transferring.
RW	I	If pull this pin high: Indicate we want to read the display data RAM or the internal state. If we force this to Low: Indicate we want to write data to display data RAM or write some internal state to registers.
CS	I	This pin is normal low clock input. Data on D0~D7 bi-direction data bus are latched at the falling edge of CS
D0~D7	B	Those bi-direction pins are used for DATA or command transferring.
CE	I	High input to this pin to enable the control pins on the driver.
OSC1	I	Oscillator input pin. For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins. For external oscillator mode, OSC1 pin should be left open
OSC2	O	Oscillator output pin For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. External Oscillator input For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.
C1P, C1N	—	If internal DC/DC converter is enabled, a capacitor is required to connect these two pins.
C2P, C2N	—	If internal tripler is enabled, a capacitor is required to connect these two pins. Otherwise, leave these pin open.
VLL2~VLL6	O	Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal voltage divider enable, a 0.1μF capacitor to VSS is required on each pin.
DUM1, DUM2	O	If internal voltage divider is enable with 1/7 bias selected, a capacitor to VSS is required on each pin. Otherwise, pull these two pin to VSS
C+, C-	—	If internal divider circuit is enable, a capacitor is required to connect between these two pin
VCCA1	O	If internal DC/DC Converter is enabled, a 0.1μF capacitor from this pin to VSS is required. It can also be an external bias input pin if internal DC/DC converter is not used
VF, VR	—	This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and VSS, a 10uF capacitor placed between VR and VSS.
COM0~COM32	O	These pins provide the row driving signal to LCD panel
VDDA	I	VDDA is the positive supply to the noise sensitive circuitry and must have same voltage level with VDD
ICON1~ICON4	O	There are four independent annunciator driving outputs
IBP	O	This pin combines with ICON1~ICON4 pins to form annunciator driving part.
SEG0~SEG119	O	These 120 pins provide LCD column driving signal to LCD panel.

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 4.0V
Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V
LCD Input Voltage.....–0.3V to 10.5V
Storage Temperature .....–65°C to 150°C
Operating Temperature .....–30°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

HT0610 contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precaution to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit . For proper operation it is recommended that V_{IN} and Vout be constrained to the range VSS < or = (V_{IN} or V_{OUT}) < or = VDD. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either VSS or VDD). Unused outputs must be left open. This device may be light sensitive? caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Supply voltage							
V_{DD}	Operating Voltage	2.4V~3.5V	VDDA=VDD	2.4	3.15	3.5	V
Supply Current							
I_{RW}	Read/write Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Measure with VDD fixed at 3.15V Internal DC/DC converter on, display on, tripler enable, read/write accessing, t_{CYC}=1MHz, Osc freq.=50kHz, 1/33 duty, 1/7 bias	120	170	200	μA
I_{ON1}	Display on Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Internal DC/DC converter on, display on, tripler enable, read/write HALT, Osc freq.=50kHz, 1/33 duty, 1/7 bias	130	110	140	μA
I_{ON2}	Display on Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Internal DC/DC converter on, display on, tripler enable, read/write HALT, Osc freq.=38.4kHz, 1/33 duty, 1/7 bias	140	100	120	μA
I_{STB1}	Standby Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Display off, oscillator disabled, read/write HALT	—	300	500	nA
I_{STB2}	Standby Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Display off, oscillator enabled, read/write HALT, external oscillator and frequency=50kHz	—	0.6	1	μA
I_{STB3}	Standby Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Display off, oscillator enabled, read/write HALT, internal oscillator and frequency=50kHz	—	23	30	μA
I_{ICON}	Standby Mode Supply Current Drain from Pin VDDA and VDD	2.4V~3.5V	Low power I_{CON} mode, oscillator enable, read/write HALT, internal oscillator and frequency=50kHz	—	25	30	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
VLCD voltage (Absolute value referenced to VSS)							
V_{LCC1}	LCD Driving Voltage Generator Output Voltage at Pin VCCA1	2.4V~3.5V	Display on, internal DC/DC converter enable, tripler enable, oscillator and frequency=50kHz, regulator enable, divider enable I_{OUT}≤100μA	—	3×VDD	10.5	V
V_{LCC2}	LCD Driving Voltage Generator Output Voltage at Pin VCCA1	2.4V~3.5V	Display on, internal DC/DC converter enable, doubler enable, oscillator and frequency=50kHz, regulator enable, divider enable I_{OUT}≤100μA	—	2×VDD	7	V
V_{LCD}	LCD Driving Voltage Input at Pin VCCA1	2.4V~3.5V	Internal DC/DC converter disable	5	—	10.5	V
Output voltage							
V_{OH1}	Output High Voltage at Pin D0~D7, ICON1~ICON4, IBP and OSC2	2.4V~3.5V	I_{OUT}=100μA	0.8×VDD	—	VDD	V
V_{OL1}	Output Low Voltage at Pin D0~D7, ICON1~ICON4, IBP and OSC2	2.4V~3.5V	I_{OUT}=100μA	0	—	0.2×VDD	V
V_{R1}	LCD Driving Voltage Source at Pin VR	2.4V~3.5V	Regulator enable, I_{OUT}=50μA	0	—	VCCA1	V
V_{R2}	LCD Driving Voltage Source at Pin VR	2.4V~3.5V	Regulator disable	—	Floating	—	V
Input voltage							
V_{IH1}	Input High Voltage at Pin RES, CE, CS, D0~D7, RW, DCOM, OSC1 and OSC2	2.4V~3.5V	—	0.8×VDD	—	VDD	V
V_{IL1}	Input Low Voltage at Pin RES, CE, CS, D0~D7, RW, DCOM, OSC1 and OSC2	2.4V~3.5V	—	0	—	0.2×VDD	V
LCD display voltage							
V_{LL6}	LCD Driving Voltage Output from Pin VLL6~VLL2	2.4V~3.5V	1/5 bias ratio, voltage divider enable, regulator enable	—	VR	—	V
V_{LL5}		2.4V~3.5V		—	0.8×VR	—	V
V_{LL4}		2.4V~3.5V		—	0.6×VR	—	V
V_{LL3}		2.4V~3.5V		—	0.4×VR	—	V
V_{LL2}		2.4V~3.5V		—	0.2×VR	—	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{LL6}		2.4V~3.5V	1/7 bias ratio, voltage divider enable, regulator enable	—	VR	—	V
V_{LL5}		2.4V~3.5V		—	6/7×VR	—	V
V_{LL4}		2.4V~3.5V		—	5/7×VR	—	V
D_{UM2}		2.4V~3.5V		—	4/7×VR	—	V
D_{UM1}		2.4V~3.5V		—	3/7×VR	—	V
V_{LL3}		2.4V~3.5V		—	2/7×VR	—	V
V_{LL2}		2.4V~3.5V		—	1/7×VR	—	V
V_{LL6}		2.4V~3.5V	External voltage generator, internal voltage divider disable	0.5×VCCA1	—	VCCA1	
V_{LL5}		2.4V~3.5V		0.5×VCCA1	—	VCCA1	
V_{LL4}		2.4V~3.5V		0.5×VCCA1	—	VCCA1	
V_{LL3}		2.4V~3.5V		vss	—	0.5×VCCA1	
V_{LL2}		2.4V~3.5V		vss	—	0.5×VCCA1	
Output Current							
I_{OH}	Output High Current Source from Pins D0~D7, ICON1~ICON4, IBP and OSC2	2.4V~3.5V	V_{OUT}=VDD−0.1V	—	1.5	—	mA
I_{OL}	Output Low Current Drain by Pins D0~D7, ICON1~ICON4, IBP and OSC2	2.4V~3.5V	V_{OUT}=0.1V	—	5	—	mA
I_{OZ}	Output Tri-state Current Drain Source at Pins D0~D7 and OSC2	2.4V~3.5V	—	−1	—	1	μA
I_{IL}/I_{IH}	Input Current at Pins RES, CE, CS, D0~D7, RW, DCOM, OSC1 and OSC2	2.4V~3.5V	—	−1	—	1	μA
On resistance							
R_{ON}	Channel Resistance between LCD Driving Signal Pins (Segment and Common) and Driving Voltage Input Pins (VLL2 to VLL6)	2.4V~3.5V	During display on, 0.1V apply between two terminals, VCCA1 within operating voltage range	—	—	5	kΩ
V_{MR}	Memory Retention Voltage (VDD) Standby Mode, Retained All Internal Configuration and BGDRAM Data	2.4V~3.5V	—	1.8	—	—	V
C_{IN}	Input Capacitance All Control Pins	2.4V~3.5V	—	—	5	7.5	pF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Temperature coefficient compensation							
PTC0	Flat Temperature	2.4V~3.5V	TC1=0, TC2=0, regulator disable	—	0	—	%
PTC1	Coefficient	2.4V~3.5V	TC1=0, TC2=1, regulator enable	—	–0.18	—	%
PTC2	Temperature Coefficient 1*	2.4V~3.5V	TC1=1, TC2=0, regulator enable	—	–0.22	—	%
PTC3	Temperature Coefficient 2* Temperature Coefficient 3*	2.4V~3.5V	TC1=1, TC2=1, regulator enable	—	–0.35	—	%
V_{CON}	Internal Contrast Control VR Output Voltage with Internal Contrast Control Selected 16 Voltage Levels Controlled by Software Each Level is Typical of 2.25% of the Regulator Output Voltage	2.4V~3.5V	Internal regulator enabled, internal contrast control enabled	—	±18	—	%
Oscillator frequency							
F_{OSC1}	Oscillator Frequency of Display Timing Generator with 60Hz Frame Frequency	2.4V~3.5V	Set clock frequency to slow	—	38.4	—	kHz
F_{OSC2}	Oscillator Frequency of Display Timing Generator with 60Hz Frame Frequency	2.4V~3.5V	Set clock frequency to normal	—	50	—	kHz
F_{ICON1}	Four Static ICON Display (50% Duty Cycle) from Pins ICON1~ICON4 and IBP	2.4V~3.5V	—	—	18.75	—	Hz
F_{ICON2}	Four Static ICON Display (50% Duty Cycle) from Pins ICON1~ICON4 and IBP	2.4V~3.5V	—	—	24.4	—	Hz
F_{FRAME1}	LCD Driving Signal Frame Frequency	2.4V~3.5V	Either external clock input or internal oscillator enable, either 1/32 or 1/16 duty cycle, graphic display mode	—	66	—	Hz
F_{FRAME2}	LCD Driving Signal Frame Frequency	2.4V~3.5V	Either external clock input or internal oscillator enable, either 1/32 or 1/16 duty cycle	—	65	—	Hz
F_{CON1}	LCD Driving Signal Frame Frequency	2.4V~3.5V	Either external clock input or internal oscillator enable, 1/33 duty cycle, graphic display mode	—	64	—	Hz
F_{CON2}	LCD Driving Signal Frame Frequency	2.4V~3.5V	Either external clock input or internal oscillator enable, 1/33 duty cycle	—	63	—	Hz
Internal oscillation frequency							
O_{SC}	Internal OSC Oscillation Frequency with Different Value of Feedback Resistor	2.4V~3.5V	Internal oscillator enable within operation range	See the figure as follow			

Note:

* The formula for the temperature coefficient is: $TC\ (\%)=\frac{VR\ at\ 50^{\circ}C - VR\ at\ 0^{\circ}C}{50^{\circ}C - 0^{\circ}C}\times\frac{1}{VR\ at\ 25^{\circ}C}\times 100\%$

Total variation of VR ΔV_{RT} is affected by the following factors:

Process variation of regulator ΔV_R

External VDD variation contributed to regulator ΔV_{VDD}

External resistor pair Ra/Rf contributed to regulator ΔV_{RES}

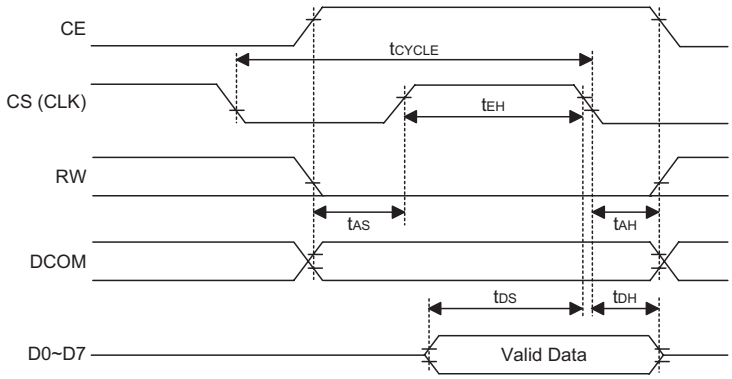
Where $\Delta V_{RT} = \sqrt{\Delta V_R^{\ 2} \quad \Delta V_{VDD}^{\ 2} \quad \Delta V_{RES}^{\ 2}}$

Assume external VDD variation is ±6% at 3.15V and 1% variation resistor used at application

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{RES} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

Parallel timing characteristics (Write cycle) Ta=30°C~85°C, DV_{DD}=2.4V~3.5V, V_{SS}=0V

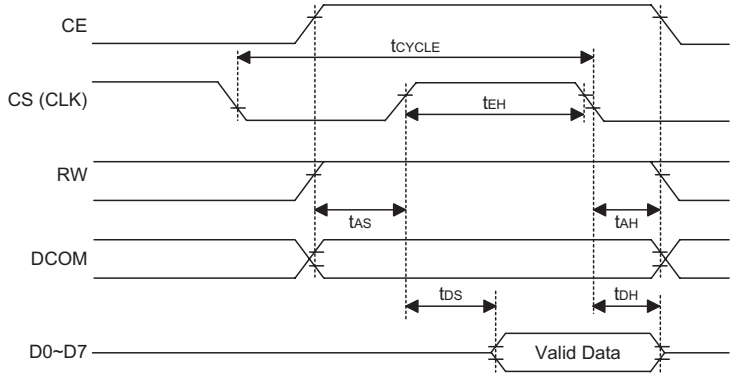
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CYCLE}	Enable Cycle Time	620	—	—	ns
t_{EH}	Enable Pulse Width	300	—	—	ns
t_{AS}	Address Setup Time	10	—	—	ns
t_{DS}	Data Setup Time	300	—	—	ns
t_{DH}	Data Hold Time	30	—	—	ns
t_{AH}	Address Hold Time	30	—	—	ns



Timing characteristics (Write cycle)

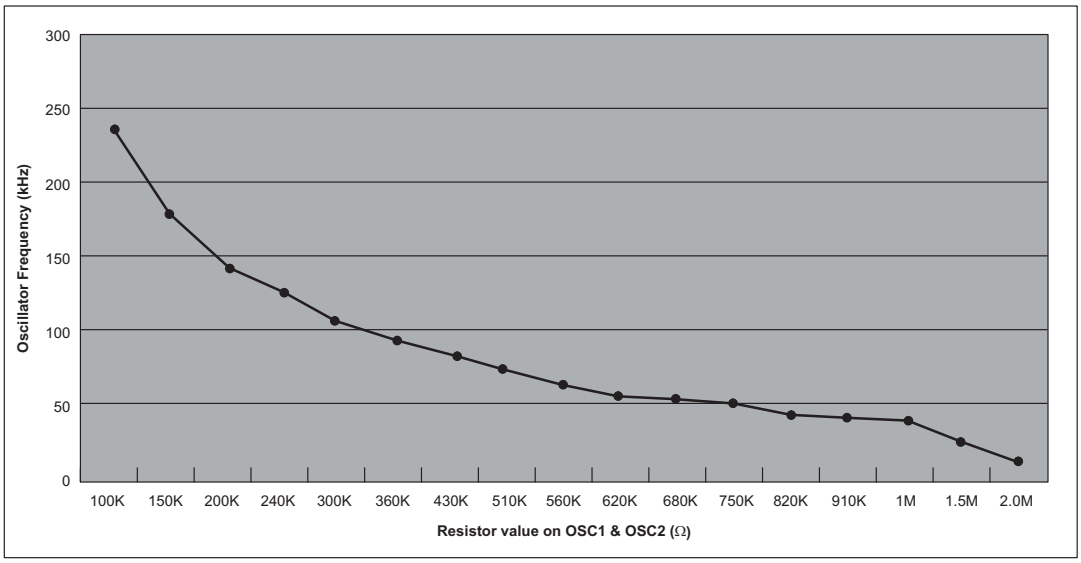
Parallel timing characteristics (Read cycle) Ta=30°C~85°C, DV_{DD}=2.4V~3.5V, V_{SS}=0V

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CYCLE}	Enable Cycle Time	620	—	—	ns
t_{EH}	Enable Pulse Width	300	—	—	ns
t_{AS}	Address Setup Time	10	—	—	ns
t_{DS}	Data Setup Time	—	—	300	ns
t_{DH}	Data Hold Time	10	—	—	ns
t_{AH}	Address Hold Time	30	—	—	ns



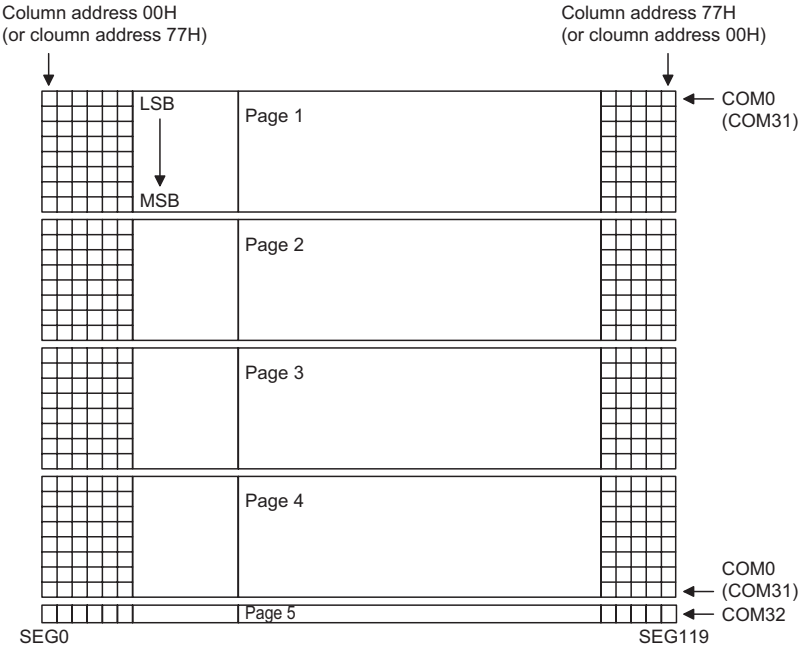
Timing characteristics (Read cycle)

Functional Description



Internal oscillator frequency relationship with different external resistor value

- Set clock frequency to slow: $F_{FRAME1}=F_{OSC1}/576$
- Set clock frequency to normal: $F_{FRAME2}=F_{OSC2}/768$



Built-in graphic display data RAM (BGDRAM) address map

Command	Description
Set Display On/Off (Display Mode/Standby Mode)	The display on command turns the LCD common and segment outputs on and has no effect to the static icons output. This command causes the conversion of data in BGDRAM to necessary waveforms on the common and segment driving outputs. The on-chip bias generator is also turned on by this command. (Note: ″oscillator on″ command should be sent before ″display on″ is selected.) The display off command turns the display off and the states of the LCD driver are as follow during display off: • The common and segment outputs are fixed at VLL1(VSS) • The bias voltage generator is turned off. • The RAM and content of all register are retained. • IC will accept new commands and data. • The status of the static Icons and oscillator are not affected by display off command.
Set BGDRAM Page Address	This command positions the row address to 1 of 5 possible positions in BGDRAM.
Master Clear BGDRAM	This command is to clear the 480 byte BGDRAM by setting the RAM data to zero. Issue this command followed by a dummy writes command. The RAM for icon line will not be affected by this command.
Master Clear Icons	This command is used to clear the data in page 5 of BGDRAM, which stores the icon line data. Before using this command, set the page address to page 5 by the command ″set BGDRAM page address″. A dummy write data is also needed after this ″master clear Icons″ command to make the clear icon action effective.
Set Display with Icon Line	If 1/32 Mux selected, use this command change to 1/33 Mux for using the Icon line. This command can also change Icon display mode to normal display mode (1/32 or 1/33 MUX).
Set Icon Display Mode	This command forces the output to the icon display mode. Display on row 0 to row 31 will be disabled.
Set Icon Line/Static Icon Contrast Level	The contrast of the icon line and static icon in icon mode can be set by this command. There are four levels to select from.
Set Vertical Scroll Value	This command is used to scroll the screen vertically with scroll value 0 to 31. With scroll value equals to 0, row 0 of BGDRAM is mapped to com 0 and row 1 through row 31 are mapped to com 1 through com 31 respectively. With scroll value equal to 1, row 1 of BGDRAM is mapped to com 0, then row 2 through row 31 will be mapped to com 1 through com 30 respectively and row 0 will be mapped to com 31. Com 32 is not affected by this command.
Save/Restore BGDRAM Column Address	With bit option=1 in this command, the save/restore column address command saves a copy of the column address of BGDRAM. With a bit option=0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.
Set Column Mapping	This instruction selects the mapping of BGDRAM to segment drivers for mechanical flexibility. There are 2 mappings to select: • Column 0~column 119 of BGDRAM mapped to SEG0~SEG119 respectively • Column 0~column 119 of BGDRAM mapped to SEG119~SEG0 respectively COM 32 will not be affected by this command. Detailed information please refer to section ″display output description″.
Set Row Mapping	This instruction selects the mapping of BGDRAM to common drivers for mechanical flexibility. There are 2 mappings to select: • Row 0~Row 31 of BGDRAM mapped to COM 0~COM 31 respectively. • Row 0~Row 31 of BGDRAM mapped to COM 31~COM 0 respectively. COM 32 will not be affected by this command. Detail information please refer to section ″display output description″.

Command	Description
Set Static Icon Control Signal	This command is used to control the active states of the 4 stand-alone icons drivers.
Set Oscillator Disable/Enable	This command is used to either disable or enable the oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command ″set display on/off″ and ″set static Icon control signal″. Refer to command ″set internal/external oscillator″ for more information.
Set Internal/External Oscillator	This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leaves OSC1 open.
Set Clock Frequency	Use this command to choose from two different oscillation frequency (50kHz or 38.4kHz) to get the 60Hz frame frequency. With frequency high, 50kHz clock frequency is preferred. 38.4kHz clock frequency (low frequency) enable for power saving purpose.
Set DC/DC Converter On/Off	Use this command selects the internal DC/DC converter to generate the VDDA1 from VDD. Disable the internal DC/DC converter if external VCCA1 is provided.
Set Voltage Doubler/Tripler	Use this command to choose doubler or tripler when the internal DC/DC converter is enabled.
Set Internal Regulator On/Off	Choose bit option 0 to disable the internal regulator. Choose bit option 1 to enable internal regulator, which consists of the internal contrast control and temperature compensation circuits.
Set Internal Voltage Divider On/Off	If the internal voltage divider is disabled, external bias can be used for VLL6 to VLL2. If the internal voltage divider is enabled, the internal circuit will automatically select the correct bias level according to the number of multiplex. Refer to command ″bias ratio select″.
Set Duty Cycle	This command is to select 16 mux or 32 mux display. When 16 mux is enabled, the unused 16 common outputs will be swinging between VLL2 and VLL5 for dummy scan purpose and doubler will be used.
Set Bias Ratio	This command sets the 1/5 bias or 1/7 bias for the divider output. The selection should match the characteristic of LCD panel.
Set Internal Contrast Control On/Off	This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option=1, the software selection for delta bias voltage control is enabled. With bit option=0, internal contrast control is disabled.
Increase/Decrease Contrast Level	If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after power on reset.
Set Contrast Level	This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use.
Read Contrast Value	This command allows the user to read the current contrast level value. With RW input HIGH (READ), DCOM input LOW (Command) and D7, D6, D5 and D4 are equal to 0001, the value if the internal contrast value can be read on D0~D3 at the falling edge of CS.
Set Temperature Coefficient	This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in electrical characteristics table.
Set IDD Reduction Mode On/Off	By using this command to reduce the display clock frequency by HALT. Use in Icon mode to reduce standby current

Command table

Bit Pattern (D7~D0)	Command	Comment
$00000X_2X_1X_0$	Set BGDRAM Page Address	Set BGDRAM page address using $X_2X_1X_0$ as address bits. $X_2X_1X_0$=000: page 1 (POR; initial state) $X_2X_1X_0$=001: page 2 $X_2X_1X_0$=010: page 3 $X_2X_1X_0$=011: page 4 $X_2X_1X_0$=100: page 5
$000011X_1X_0$	Set Icon Line/Annunciator Contrast Level	Set one of the 4 available values to the icon and annunciator contrast, using X_1X_0 as data bits. X_1X_0=00 (Von=0.87VDD) X_1X_0=01 (Von=0.71VDD) X_1X_0=10 (Von=0.61VDD) (POR initial state) X_1X_0=11 (Von=0.55VDD)
$0001X_3X_2X_1X_0$	Set Contrast Level	Set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR
$0001X_3X_2X_1X_0$	Read Contrast Value	With DCOM pin input low, RW pin input high, and D7~d4 pins equal to 0001 at the rising edge of CS, the value of the internal contrast register will be latched out at D3, D2, D1 and D0 pins, i.e. $X_3X_2X_1X_0$ at the rising edge of CS.
$0010000X_0$	Set Voltage Doubler/Tripler	X_0=0: Select voltage tripler (POR initial state) X_0=1: Select voltage doubler
$0010001X_0$	Set Column Mapping	X_0=0: COL0 to SEG0 (POR initial state) X_0=1: COL0 to SEG119
$0010010X_0$	Set Row Mapping	X_0=0: ROW0 to COM0 (POR initial state) X_0=1: ROW0 to COM31
$0010011X_0$	Reserved	
$0010100X_0$	Set Display On/Off	X_0=0: Display off (POR initial state) X_0=1: Display on
$0010101X_0$	Set DC/DC Converter On/Off	X_0=0: DC/DC converter off (POR initial state) X_0=1: DC/DC converter on
$0010110X_0$	Set Internal Regulator On/Off	X_0=0: Internal regulator off (POR initial state) X_0=1: Internal regulator on When the application employs external contrast control, the internal contrast control, temperature compensation and the regulator must be enabled.
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal voltage divider off (POR initial state) X_0=1: Internal voltage divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal contrast control off (POR initial state) X_0=1: Internal contrast control on Internal contrast circuits can be disabled if external contrast circuit is preferred.
$0011001X_0$	Set Clock Frequency	X_0=0: Low frequency (38.4kHz) (POR initial state) X_0=1: High frequency (50kHz)
$0011010X_0$	Save/Restore RAM Column Address	X_0=0: Restore address X_0=1: Save address
00110110	Master Clear RAM	Master clear BGDRAM page 1 to 4
00110111	Master Clear Icons	Master clear of BGDRAM page 5

Bit Pattern (D7~D0)	Command	Comment
0011100X_0	Set Bias Ratio	X_0=0: Set 1/7 bias (POR initial state) X_0=1: Set 1/5 bias
0011101X_0	Reserved	X_0=0: Normal operation (POR initial state) X_0=1: Test mode (Note: make sure to set X_0=0: during application)
0011110X_0	Set Display with Icon Line	X_0=0: Set display mode without Icon line (POR initial state) X_0=1: Set display mode with Icon line
00111110	Set Icon Display Mode	Power saving icon display mode, COM 0 to COM 31 will be disabled.
010$X_4X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_4X_3X_2X_1$ as number for lines to scroll. Scroll value=0 upon POR
01100$A_1A_0X_0$	Set Static Icon Control Signals	A_1A_0=00: Select Icon 1 (POR initial state) A_1A_0=01: Select Icon 2 A_1A_0=10: Select Icon 3 A_1A_0=11: Select Icon 4 X_0=0: Turned selected Icon off (POR state) X_0=1: Turned selected Icon on
0110100X_0	Set Duty Cycle	X_0=0: 1/32 duty and triple enabled (POR initial state) X_0=1: 1/16 duty and doubler enabled
0110101X_0	Set IDD Reduction Mode	X_0=0: Normal mode X_0=1: I_{DD} reduction mode
011011X_1X_0	Set Temperature Coefficient	X_0=00: 0.00% (POR initial state) X_0=01: −0.18% X_0=10: −0.22% X_0=11: −0.35%
0111000X_0	Increase/Decrease Contrast Value	X_0=0: Decrease by one level (POR initial state) X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
0111001X_0	Reserved	
0111010X_0	Reserved	
0111011X_0	Reserved	X_0=0: Normal operation (POR initial state) X_0=1: Test mode select (Note: make sure to set X_0=0 during application)
0111100X_0	Reserved	
0111101X_0	Set Internal/External Oscillator	X_0=0: Internal oscillator (POR initial state) X_0=1: External oscillator If resistors are placed at OSC1 and OSC2. For external oscillator, simply feed clock in OSC2.
0111110X_0	Reserved	
0111111X_0	Set Oscillator Disable/Enable	X_0=0: Oscillator disable (POR initial state) X_0=1: Oscillator enable This is the master control for oscillator circuitry. This command should be issued after the ″external/internal oscillator″ command.
1$X_6X_5X_4X_3X_2X_1X_0$	Set BGDRAM Address	Set BGDRAM column address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits

Data read write

- To read data from the BGDRAM, input high to RW pin and DCOM pin. Data is valid at the falling edge of CS. And the BGDRAM column address pointer will be increased by one automatically.
- To write data to the BGDRAM, input low to RW pin and high to DCOM pin. Data is latched at the falling edge of CS. And the BGDRAM column address pointer will be increased by one automatically.
- No auto address pointer increment will be performed for the dummy write data after ″master clear BGDRAM″

Address increment table (Automatic)

DCOM	RW	Comment	Address Increment	Note
0	0	Write command		
0	1	Read command		*1
1	0	Write data	√	*2
1	1	Read data	√	

Address increment is done automatically data read write. The column address pointer of BGDRAM*3 is affected.

Note: ″*1″ Refer to the command read contrast value

″*2″ If write data is issued after command clear RAM, address increase is not applied

″*3″ Column address will be wrapped around when overflow

Power up sequence (Command required)

Command Required	POR Status	Note
Set Clock Frequency	Low	*1
Set Oscillator Enable	Disable	*1
Set Static Icon Control Signals	Static Icon off	*1
Set Duty Cycle	1/32 duty	*1
Set Bias Ratio	1/7 bias	*1
Set Internal DC/DC Converter On	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Increase Contrast Level	Contrast level=0	*1, *2, *3
Set Internal Voltage Divider On	Off	*1
Set Segment Mapping	SEG0=COLUMN0	
Set Common Mapping	COM0=ROW0	
Set Vertical Scroll Value	Scroll value=0	
Set Display On	Off	

Note: ″*1″ Required only if desired status differ from power on reset

″*2″ Effective only if internal contrast control is enabled.

″*3″ Effective only if the regulator is enabled.

Command Required for Display Mode Setup

Display Mode	Command Required
Display Mode	Set external/internal oscillator* Set oscillator enable* Set display on*
Static Icon Display	Set external/internal oscillator* Set oscillator enable* Set static Icon control signal*
Standby Mode 1	Set display off* Set oscillator disable*
Standby Mode 2	Set external oscillator* Set static Icon control signal* Set display off* Set oscillator enable*
Standby Mode 3	Set internal oscillator* Set static Icon control signal* Set display off* Set oscillator enable*

Other related command with display mode: set duty cycle, set column mapping, set row mapping, set vertical scroll value.

Command Related to Internal DC/DC Converter

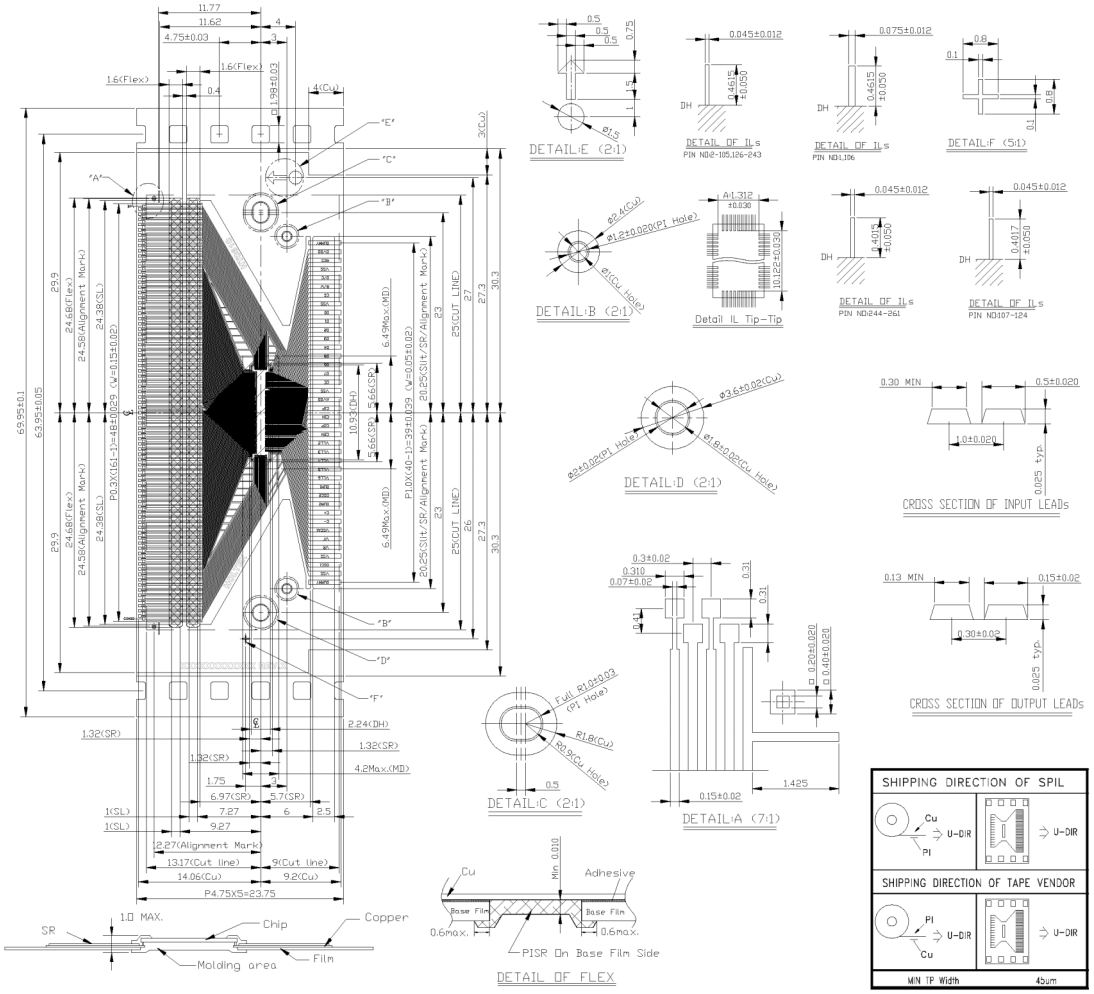
Set oscillator disable/enable, set internal regulator on/off, set duty cycle, set temperature coefficient, set internal contrast control on/off, increase contrast level, set internal voltage divider on/off, set bias ratio, set display on/off, set internal/external oscillator, set contrast level, set voltage doubler/tripler, set 33 mux display mode, set Icon display mode.

* You do not need to resend the command again if it is set previously.

Command Required for R/W Actions on RAM

R/W Actions on RAM	Command Required
Read data from BGDRAM Write data to BGDRAM	Set BGDRAM page address* Set BGDRAM column address* Read/write data
Save or restore BGDRAM column address	Save or restore BGDRAM column address
Increase BGDRAM address by one	Dummy read data
Master clear BGDRAM	Master clear BGDRAM Dummy write data

* You do not need to resend the command again if it is set previously.



Note: Film: UPILEX-S 75±5μm thickness
Copper: FQ-VLP 25±5μm thickness
Adhesive: Toray #7100, 12±2μm thickness
Solder resist: AE-70-M11, 26±14μm thickness
Flex coating: FS-100L Min. 10μm

Plating: Sn 0.21±0.05μm thickness

All corner radii of base film are less than 0.2mm unless otherwise noted

Other specs than display in this drawing are based on the standard spec lists

All dimensional tolerances of "SR" & "Flex" are ±0.2mm & 0.3mm unless otherwise noted

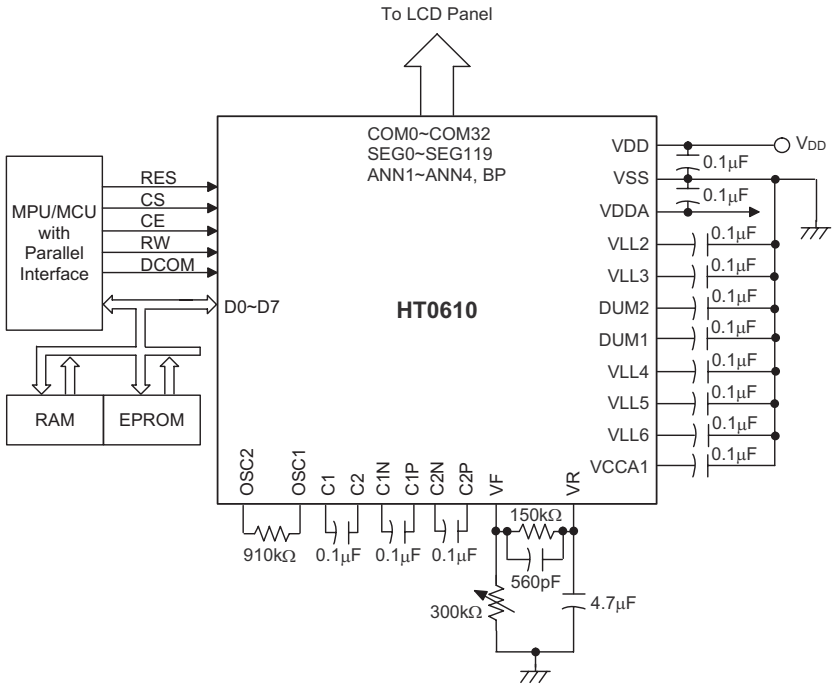
All dimensional tolerances of "base film" are ±0.05mm unless otherwise noted

Inner lead accumulative pitch:
Output side: 9.359±0.008mm
Input side: 9.077±0.008mm

Reel size: Φ405mm

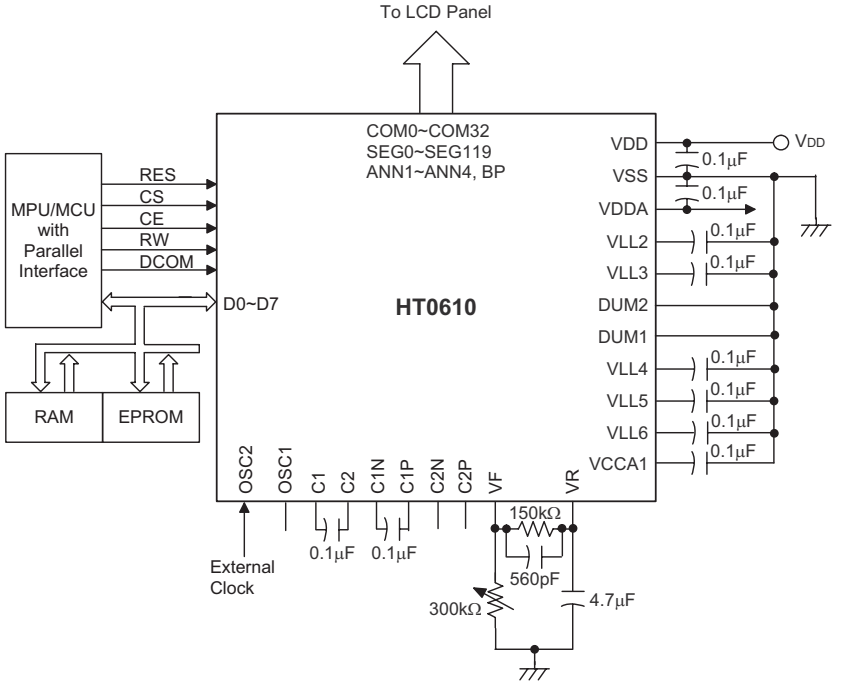
Application Circuits

32/33 MUX display with analog circuitry enabled, tripler enabled and 1/7 bias



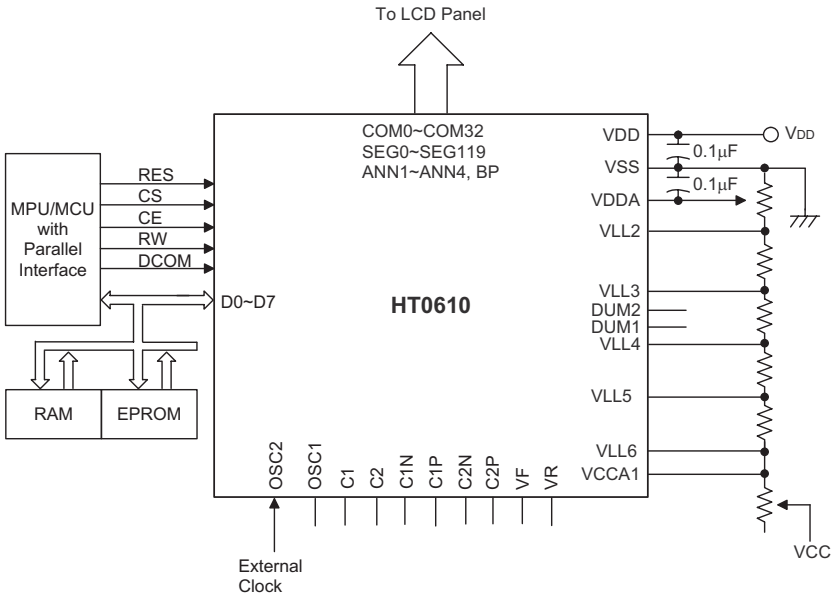
Note: VR and VF can be left open when Regulator is disabled.

16 MUX display with analog circuitry enabled, tripler enabled and 1/5 bias



Note: VR and VF can be left open when Regulator is disabled.

16/32/33 MUX display with analog circuitry disabled



Note: VR and VF can be left open when Regulator is disabled.

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