HT16014

80 Segment Dot Matrix LCD Driver

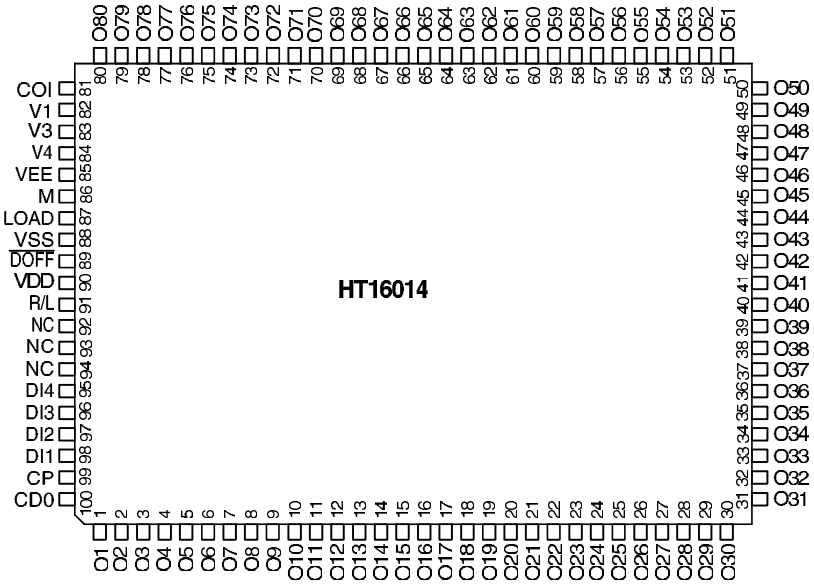
Features

- Dot matrix 80 segment driver
- operating voltage: 10V~30V (V_{DD}~V_{EE})
- Power supply for logic circuit from 2.7V to 5.5V
- Application LCD duty selection from 1/64 to 1/256
- 80 internal LCD driver circuit
- Data transfer rate: 6.0 MHz
- 4-bit data format, bidirectional shift data transfer
- Provide chip disable pin to reduce power consumption
- CMOS process
- Pin Compatible with 79401D

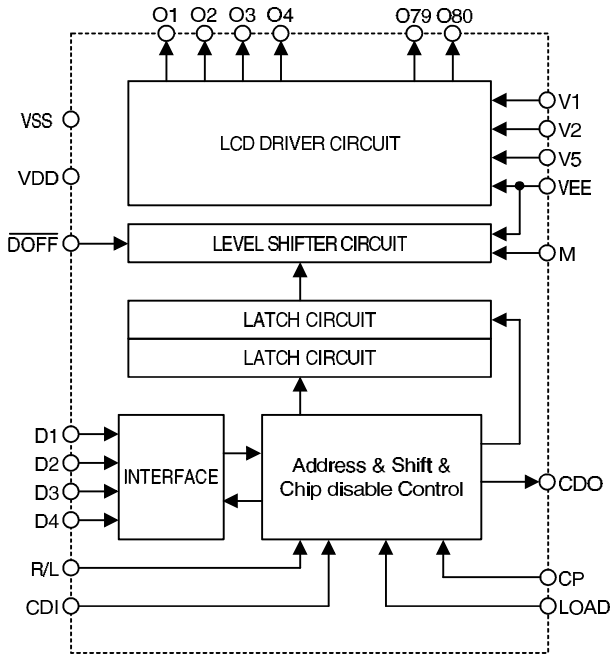
General Description

The HT16014 is a dot matrix LCD's segment driver LSI implemented in CMOS technology. The HT16014 is used for large scale dot matrix LCD panel. It is very suitable for use in portable battery drive equipment utilizing the liquid crystal display low power consumption.

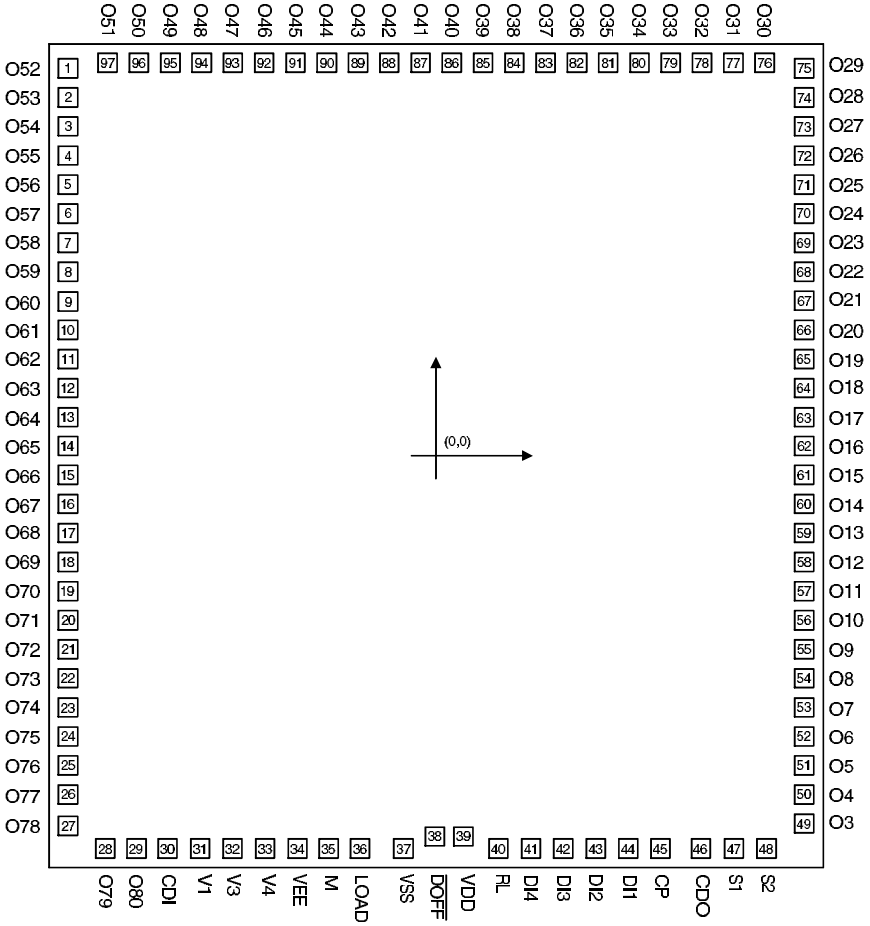
Pin Assignment



Block Diagram



Pad Assignment



Chip size: 3550 × 3890 (μm)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1647.00	1733.75	50	1647.00	–1516.25
2	–1647.00	1603.75	51	1647.00	–1386.25
3	–1647.00	1473.75	52	1647.00	–1256.25
4	–1647.00	1343.75	53	1647.00	–1126.25
5	–1647.00	1213.75	54	1647.00	–996.25
6	–1647.00	1083.75	55	1647.00	–866.25
7	–1647.00	953.75	56	1647.00	–736.25
8	–1647.00	823.75	57	1647.00	–606.25
9	–1647.00	983.75	58	1647.00	–476.25
10	–1647.00	563.75	59	1647.00	–346.25

Pad No.	X	Y	Pad No.	X	Y
11	–1647.00	433.75	60	1647.00	–216.25
12	–1647.00	303.75	61	1647.00	–86.25
13	–1647.00	173.75	62	1647.00	43.75
14	–1647.00	43.75	63	1647.00	173.75
15	–1647.00	–86.25	64	1647.00	303.75
16	–1647.00	–216.25	65	1647.00	433.75
17	–1647.00	–346.25	66	1647.00	563.75
18	–1647.00	–476.25	67	1647.00	693.75
19	–1647.00	–606.25	68	1647.00	823.75
20	–1647.00	–736.25	69	1647.00	953.75
21	–1647.00	–866.25	70	1647.00	1083.75
22	–1647.00	–996.25	71	1647.00	1213.75
23	–1647.00	–1126.25	72	1647.00	1343.75
24	–1647.00	–1256.25	73	1647.00	1473.75
25	–1647.00	–1386.25	74	1647.00	1603.75
26	–1647.00	–1516.25	75	1647.00	1733.75
27	–1647.00	–1656.25	76	1470.00	1758.75
28	–1481.00	–1758.75	77	1330.00	1758.75
29	–1341.00	–1758.75	78	1190.00	1758.75
30	–1201.00	–1758.75	79	1050.00	1758.75
31	–1056.00	–1758.75	80	910.00	1758.75
32	–911.00	–1758.75	81	770.00	1758.75
33	–766.00	–1758.75	82	630.00	1758.75
34	–621.00	–1758.75	83	490.00	1758.75
35	–481.00	–1758.75	84	350.00	1758.75
36	–341.50	–1758.75	85	210.00	1758.75
37	–147.00	–1758.75	86	70.00	1758.75
38	–6.50	–1704.75	87	–70.00	1758.75
39	123.50	–1704.75	88	–210.00	1758.75
40	279.50	–1758.75	89	–350.00	1758.75
41	424.50	–1758.75	90	–490.00	1758.75
42	569.50	–1758.75	91	–630.00	1758.75
43	714.50	–1758.75	92	–770.00	1758.75
44	859.50	–1758.75	93	–910.00	1758.75
45	1004.50	–1758.75	94	–1050.00	1758.75
46	1184.50	–1758.75	95	–1190.00	1758.75
47	1333.00	–1758.75	96	–1330.00	1758.75
48	1478.00	–1758.75	97	–1470.00	1758.75
49	1647.00	–1646.25			

Pad Description

Pad No.	Pad Name	I/O	Function
1~80	O1~O80	O	LCD driver outputs for
81	CDI.	I	Chip disable pin H: Data is not acquired L: Data is acquired

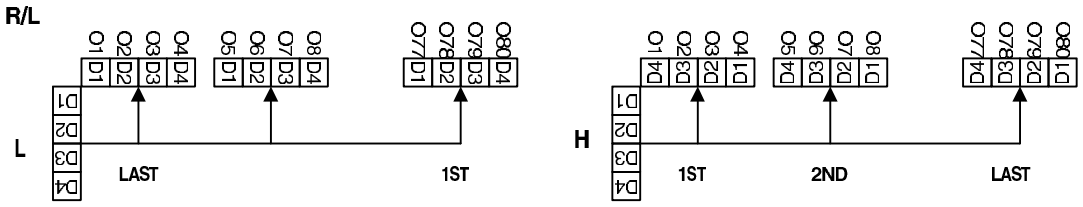
Pad No.	Pad Name	I/O	Function
82 83 84 85	V1 V3 V4 VEE	P	Power supply for LCD driver level V1 and VEE: Select level V3 and V4: Non-select level
86	M	I	Alternate signal input pad for LCD driving waveform
87	LOAD	I	Data latch clock (falling edge trigger)
88	VSS	P	Power supply for logic circuit (negative)
89	$\overline{\text{DOFF}}$	I	LCD driver output control
90	VDD	P	Power supply for logic circuit
91	R/L	I	Control the data output destination
92 93 94	NC	—	Not connected
95 96 97 98	D1 D2 D3 D4	I	Data input pin, it relation with LCD display is: DATA LCD driver output LCD display H Selected level ON L Non-selected level OFF
99	CP	I	Data acquisition clock (falling edge trigger)
100	DMIN	I	Connect the next chip with CDI pin when cascade connection is used.

Note:

LCD driver output level determined by DATA, M, $\overline{\text{DOFF}}$ pin as shown in the table:

M	DATA	$\overline{\text{DOFF}}$	OUTPUT
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	VEE
Don't care	Don't care	L	V1

LCD drive output control table:



Absolute Maximum Ratings

Supply Voltage ..... –0.3V~6.5V
Input Voltage ..... V_{SS}–0.3V~V_{DD}+0.3V
Storage Temperature ..... –40°C~125°C
Operating Temperature ..... –20°C~75°C

DC Characteristics (Condition at Ta=–20 to 75°C, V_{SS}=0V)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.7	—	5.5	V
V_{DD}~V_{EE}	Operating Voltage (LCD)	—	—	12	—	30	V
I_{GND}	Operating current1	5V	No load*	—	—	2.0	mA
I_{VEE}	Operating current2	5V	No load*	—	—	0.4	mA
I_{STB1}	Stand-by current1	5V	No load*	—	—	100	μA
I_{STB2}	Stand-by current2	5V	No load**	—	—	1	μA
V_{IH}	Input "H" level voltage	5V	—	0.7V_{DD}	—	—	V
V_{IL}	Input "L" level voltage	5V	—	—	—	0.3V_{DD}	V
I_{OH}	Output source current	5V	VOH=4.5V	0.5	—	—	mA
I_{OL}	Output sink current	5V	VOL=0.5V	0.5	—	—	mA
R_{ON}	Drive ON resistance O1~O8	5V	V_{EE}=–10V Load current=100μA	—	—	7.5	KΩ
I_{IL1}	Input leakage1	5V	VIN=0V to V_{DD}	–1	—	1	μA
I_{IL2}	Input leakage2	5V	VIN=VEE to V_{DD}	–25	—	25	μA
t_{CP}	CP cycle time	5V	—	167	—	—	ns

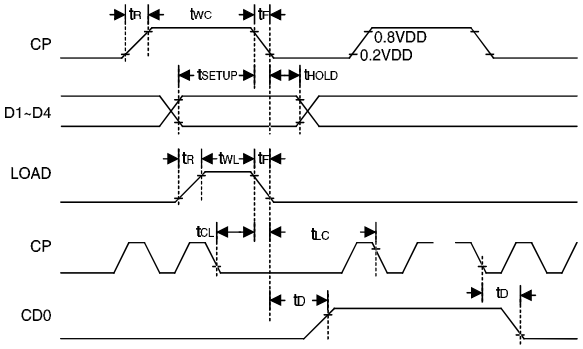
* The test conditions are listed below:
V_{DD}–V_{EE}=30V
CP=6.0MHz, f_M=35Hz
I_{GND}: currents between V_{DD} and GND
I_{VEE}: currents between V_{DD} and V_{EE}
I_{STB1}: currents between V_{DD} and GND and CDI=high

** CP=f_M=0Hz

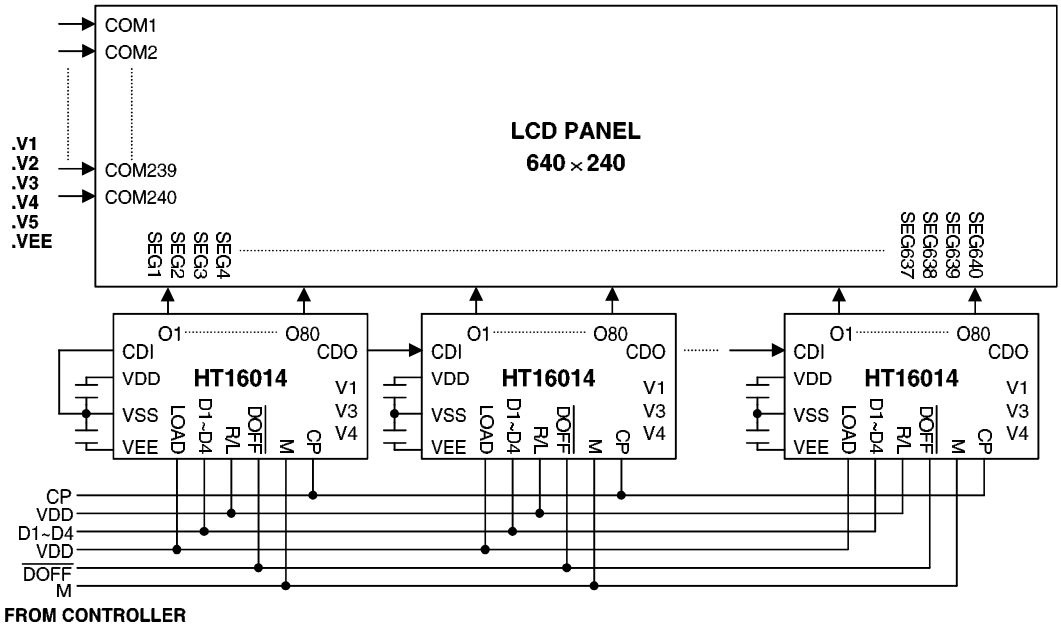
AC Characteristics at Ta=25°C, V_{SS}=0V, V_{DD}=5V±10%

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
I_{IH}	Input "H" level current	5V	—	—	—	1	μA
I_{IL}	Input "L" level current	5V	—	–1	—	—	μA
V_{OH}	Output "H" level voltage	5V	I_{OH}=–0.4mA, DIO1,DIO80	V_{DD}–0.4	—	—	V
V_{OL}	Output"L" level voltage	5V	I_{OH}=0.4mA, DIO1,DIO80	—	—	0.4	V
R_{ON}	Driver on resistor	5V	O1 to O80, V_{DD}–V_{EE}=30V, $\lvert^{*1}V_{LCD}–VO\rvert$=0.5V	—	—	3	kΩ
I_{VSS}	Power consumption (1)	5V	V_{DD}–V_{EE}=30V, CP=14KHz, No load, V_{SS}	—	—	100	μA
I_{VEE}	Power consumption (2)	5V	V_{DD}–V_{EE}=30V, CP=14KHz, No load, V_{EE}	—	—	100	ns
C_L	Input capacity	5V	CP=6MHz	—	5	—	pF
t_{SETUP}	Setup time	—	*1	30	—	—	ns
t_{HOLD}	Hold time	—	*1	30	—	—	ns
t_R	CP, LOAD rise time	—	*1	—	—	4	ns
t_F	CP, LOAD fall time	—	*1	—	—	4	ns
f_{CP}	CP (Shift clock)	3V	*1	—	—	4	MHz
		5V				6	
t_{PW}	CP (Pulse width)	—	*1	50	—	—	ns
t_D	Output delay time	5V	C_L=15pF	—	—	80	ns

*1



Application Diagram



Example of Waveform (1/240 duty, 1/16 bias)