HT1602

40 Dot Matrix LCD Segment Driver

Features

- Operating voltage: 4.5V~5.5V
- LCD driving voltage: 8V~16V
- Applicable LCD duty cycle from 1/8 to 1/64
- Suitable for various types of LCD panel
- Bias voltage adjustable from an external source

Applications

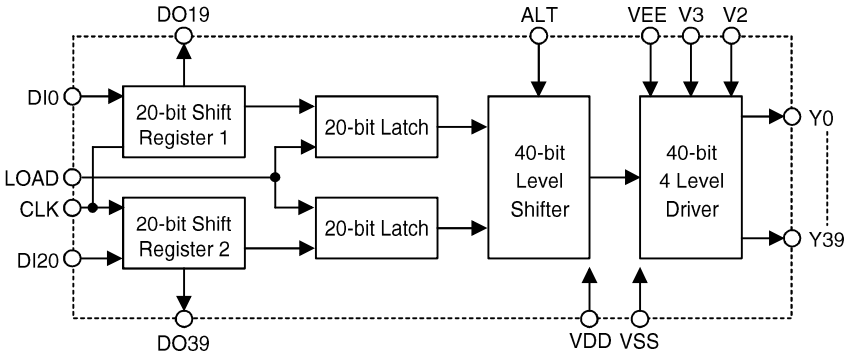
- Electrical dictionaries
- Portable computers
- Remote controllers
- Calculators

General Description

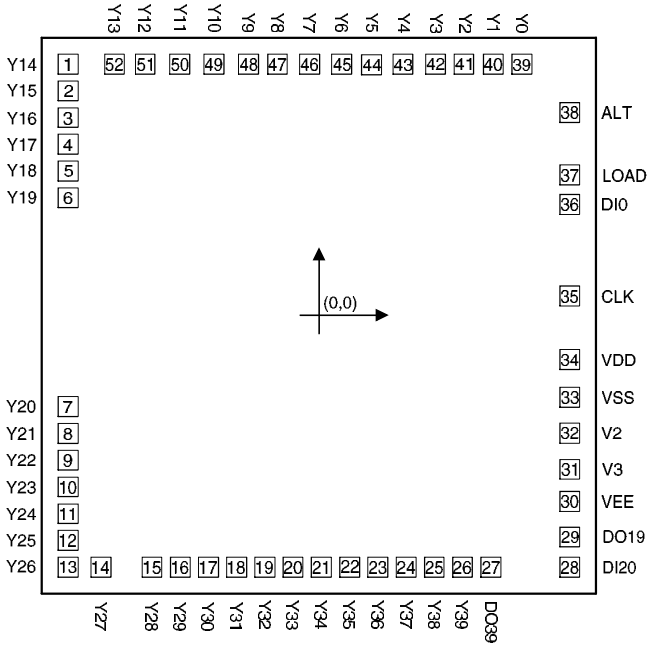
The HT1602 is a dot matrix LCD segment driver LSI implemented in the CMOS technology. It is equipped with a 40-bit shift register (two 20-bit shift registers), a 40-bit latch (two 20-bit latches), a 40-bit level shifter, a 40-bit 4-level driver, and control circuits.

The HT1602 can convert serial data received from an LCD controller to parallel data and then send them out as LCD driving waveforms to the LCD panel. The LSI can be applied up to 1/64 duty. Furthermore, the bias voltage which determines the LCD driving voltage has an option of being supplied from an external source. The chip is thus suitable for driving various types of LCD panel. These special features increase the versatility of the chip.

Block Diagram



Pad Coordinates



Chip size: 164 × 164 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Unit: µm

Pad No.	X	Y	Pad No.	X	Y	Pad No.	X	Y
1	–76.23	76.23	19	–16.61	–76.23	37	75.78	42.66
2	–76.23	68.13	20	–8.10	–76.23	38	75.78	61.56
3	–76.23	60.03	21	0.5	–76.23	39	61.20	76.23
4	–76.23	51.93	22	9.10	–76.23	40	52.56	76.23
5	–76.23	43.83	23	17.60	–76.23	41	43.65	76.23
6	–76.23	35.73	24	26.15	–76.23	42	35.10	76.23
7	–76.23	–27.63	25	34.70	–76.23	43	25.20	76.23
8	–76.23	–35.73	26	43.25	–76.23	44	15.71	76.23
9	–76.23	–43.83	27	51.89	–76.23	45	6.66	76.23
10	–76.23	–51.93	28	75.78	–76.23	46	–3.06	76.23
11	–76.23	–60.03	29	75.78	–67.14	47	–12.83	76.23
12	–76.23	–68.13	30	75.78	–56.34	48	–21.60	76.23
13	–76.23	–76.23	31	75.78	–46.62	49	–32.04	76.23
14	–66.33	–76.23	32	75.78	–35.64	50	–42.48	76.23
15	–50.81	–76.23	33	75.78	–24.75	51	–52.92	76.23
16	–42.26	–76.23	34	75.78	–13.32	52	–62.15	76.23
17	–33.71	–76.23	35	75.78	6.03			
18	–25.16	–76.23	36	75.78	33.66			

Pad Description

Pad No.	Pad Name	I/O	Note	Description
1~26	Y14~Y39	O	*	LCD driver outputs for segments
27	DO39	O		Shift register output for the 40th bit data
28	DI20	I		Data input of shift register 2
29	DO19	O		Shift register output for the 20th bit data
30	VEE	I		LCD power supply
31, 32	V3, V2	I		LCD bias supply voltage
33	VSS	I		Power supply (negative)
34	VDD	I		Power supply (positive)
35	CLK	I		Clock pulse input for the shift register
36	DI0	I		Data input of shift register 1
37	LOAD	I		Latching signal to latch shift register data
38	ALT	I		Alternate signal input for LCD driving waveforms
39~52	Y0~Y13	O	*	LCD driver outputs for segments

Note: For Y0~Y39, any of VDD, V2, V3 or VEE can be selected as a display driving source according to the combination of latched data level and ALT signal.
Refer to the following table:

Latched Data	ALT	Display Data Output Level
Hi	Hi	VEE
	Lo	VDD
Lo	Hi	V3
	Lo	V2

Absolute Maximum Ratings

Supply Voltage ..... –0.3V to 6V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature..... 0°C to 70°C

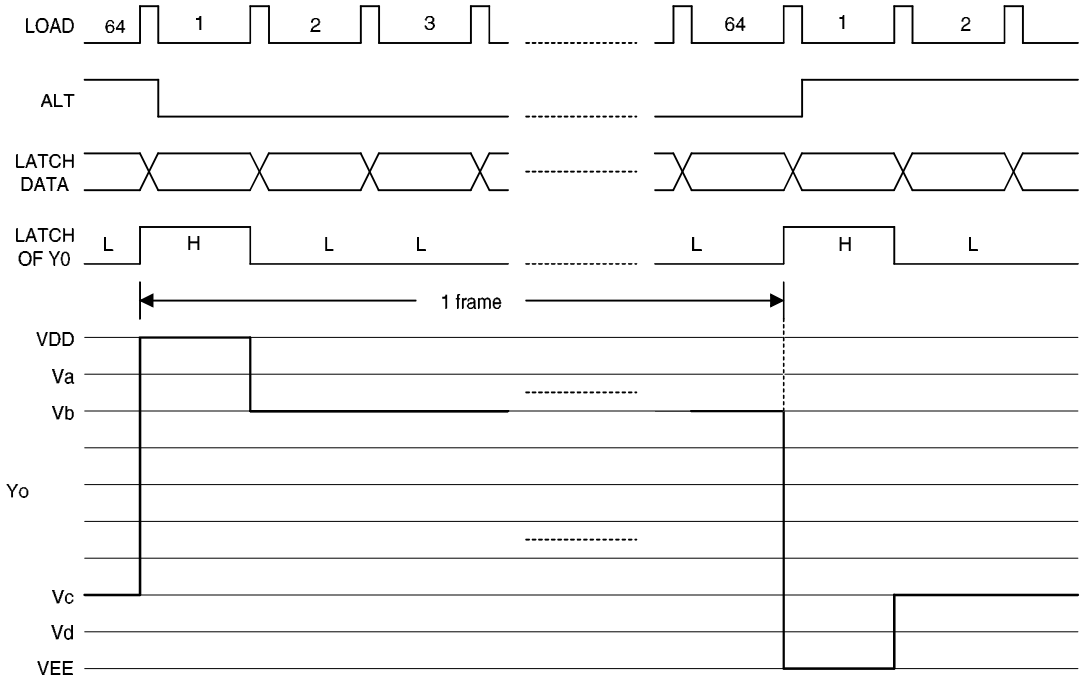
Electrical Characteristics

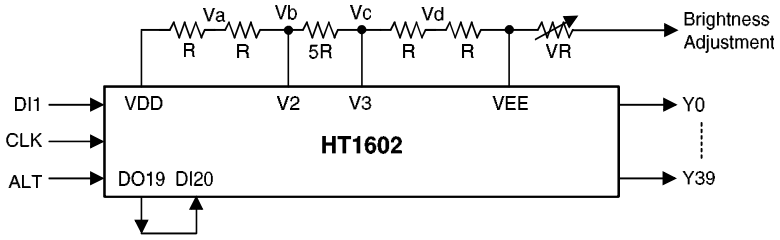
(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	4.5	—	5.5	V
I_{DD}	Operating Current	5V	No load	—	100	300	μA
I_{STB}	Stand-by Current	5V	—	—	1	5	μA
f_{LCD}	Max. Clock Frequency	5V	—	3.3	—	—	MHz
tw_{CLK}	Clock Pulse Width	5V	—	125	—	—	ns
V_{IL}	"Lo" Input Voltage	5V	—	—	—	0.2VDD	V
V_{IH}	"Hi" Input Voltage	5V	—	0.8VDD	—	—	V
V_{LCD}	LCD Driving Voltage	5V	—	8	—	16	V

Timing Diagram

1/64 duty & 1/9 bias (with the ALT changing polarity for every frame, a frame=64 commons)





Va= VDD−(1/9)VLCD
Vd= VDD−(2/9)VLCD
Vc= VDD−(7/9)VLCD
Vd= VDD−(8/9)VLCD
VEE= VDD−VLCD
VLCD= VDD−VEE; LCD driving voltage

Application Circuit

1/32 duty & 1/7 bias